REMARKS

Claims 1-21 are pending in the instant application. Claims 1-2, 5-6, 8, 10-13, 16-18, and 20-21 are amended herein. No new matter has been added as a result of the amendments.

ALLOWABLE SUBJECT MATTER

Applicant wishes to thank the Examiner for indicating that Claims 8-17 are allowable. The Office Action indicates that Claims 9-17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicant has amended independent Claim 8 to overcome the 35 U.S.C 112, second paragraph rejection, however, no new matter has been added as a result of the claim amendments. As such, Claims 8-17 are in condition for allowance and allowance of Claims 8-17 is earnestly solicited.

CLAIM OBJECTIONS

The Office Action objected to the Claims as containing informalities. The Claims have been amended herein so as to eliminate any informalities. Consequently, the Applicants respectfully request the withdrawal of the objections to the Claims.

35 U.S.C. §112 Rejections

The claims have been amended herein to obviate the rejection of Claims 5, 6, 8, 16, 17, 20 and 21 under 35 U.S.C. 112, second paragraph. Therefore, the Applicants respectfully request the withdrawal of the rejection of Claims 5, 6, 8, 16, 17, 20 and 21 under 35 U.S.C. 112, second paragraph.

Claims 5, 6, 16, 17, 20 and 21

Claims 5, 6, 16, 17, 20 and 21 have been objected to because it is purported that these claims and the specification do not provide information about the lowest and highest limits of the frequency at which the microcontroller is operating. Applicant does not fully understand the rejection because Applicant has not claimed "the highest limit" or "the lowest limit" of the frequency at which the microcontroller is operating. However, in the interest of progressing the prosecution of the instant application, Applicant has amended the Claims to include a first frequency and a second frequency to more clearly point out and distinctly claim the subject matter of the present invention. Applicant respectfully requests review and approval of these amendments.

Claim 8

Claim 8 has been amended to clearly claim that a memory of an ICE and a memory of a microcontroller are initiated. Applicant respectfully requests review and approval of these amendments.

35 U.S.C. §103 Rejection

Claims 1-7 and 18-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art in Figure 1 and pages 1-4 of Applicant's background of the invention in view of U.S. Patent No. 5,590,354 to Klapproth et al., hereafter referred to as Klapproth. The rejection is respectfully traversed for the following rational.

Applicant has reviewed the Klapproth reference and asserts that Klapproth and the claimed invention are very different. Klapproth may purport to teach a debugging environment with a microcontroller, but the microprocontroller of Klapproth is substantially different from the microcontroller of the claimed invention. For example, Claim 1 recites in part, "an ICE coupled to the computer system, wherein the ICE emulates the microcontroller, and wherein the ICE is configured to run the microcontroller code cooperatively with the microcontroller to implement the debugging process." The debugging logic of the present invention resides on the ICE and not on the microcontroller. Furthermore, the microcontroller of the present invention is a production microcontroller that does not comprise debug logic, trace buffers, and breakpoints, as does the microcontroller of Klapproth. The claimed ICE of the present invention emulates

the microcontroller and comprises the debugging logic required to debug the microcontroller.

Conversely, the microcontroller of Klapproth, as shown in Figure 1 comprises an on-chip trace memory 58, a debug support unit 56 and a processing element with caches 60 to aid in debugging. Figure 1 of Klapproth clearly shows debug logic in the microcontroller, which actually teaches away from the claimed invention that uses debug logic, resident on an ICE to perform debugging operations.

The microcontroller of the present invention does not require on-chip debugging logic or trace memories, as does the microcontroller of Klapproth because the debugging logic of the present invention is in the ICE, which allows the use of a production microcontroller for testing. Specifically, Claim 1 recites "an ICE coupled to the computer system, wherein the ICE emulates the microcontroller, and wherein the ICE is configured to run the microcontroller code cooperatively with the microcontroller to implement the debugging process." This is a very appreciable difference from the microcontroller of Klapproth, which comprises debugging logic in the microcontroller to perform debugging operations.

In addition, Claim 1 recites "enable data transmission when the microcontroller is operating at a first speed and to disable data transmission when the microcontroller is operating at a second speed." Klapproth fails to teach or suggest this limitation as claimed.

Moreover, Claim 1 recites, "wherein the ICE emulates the microcontroller." Klapproth fails to teach or suggest emulating the microcontroller on an ICE, as claimed. For this rational, Claim 1 is patentable over Applicant's admitted prior art in view of Klapproth. As such, Claim 1 is in condition for allowance and allowance of Claim 1 is earnestly solicited.

Claims 2-7 depend from independent Claim 1 and therefore, for the rational presented above, Claims 2-7 are also patentable over Applicant's admitted prior art in view of Klapproth. As such, Claims 2-7 are in condition for allowance and allowance of Claims 2-7 is earnestly solicited.

Claim 18 recites similar limitations of Claim 1. For the rational presented above, Claim 18 is patentable over Applicant's admitted prior art in view of Klapproth. As such, Claim 18 is in condition for allowance and allowance of Claim 1 is earnestly solicited.

Claims 19-21 depend from independent Claim 18 and therefore, for the rational presented above, Claims 19-21 are also patentable over Applicant's admitted prior art in view of Klapproth. As such, Claims 19-21 are in condition for allowance and allowance of Claims 19-21 is earnestly solicited.

Conclusion

In light of the above-listed remarks, the Applicant respectfully requests allowance of the remaining Claims.

The Examiner is urged to contact the Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

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